REMARKS/ARGUMENTS

Claims 1, 4, 5, 13, 14, 16, 19, 20, 28, 29, 31, 41, 42, 44, 45, 53, 54, 56, 57, 59, 60, 68, and 69 are pending in the subject application. The Examiner has rejected all of these claims under 35 U.S.C. § 103(a) as unpatentable over Sefidvash, made of record in a previous Office Action, and alternatively over Sefidvash in view of Fujimori, also made of record in a previous Office Action. Applicants respectfully traverse these rejections, and request reconsideration and allowance in view of the following arguments.

On page 5 of the Office Action, the Examiner addresses Applicants' argument regarding the claimed feature of an arbiter for receiving requests to access the volatile memory from the first bridge and second bridge and giving priority to the first bridge. Applicants had argued that giving priority to the first bridge over the second bridge only matters when there are requests coming from both bridges at the same time. The Examiner commented that the words "at the same time" are not expressly recited in the claims.

Applicants submit that that language is redundant to the priority that the claims already recite. Priority does not matter if requests are getting to a location sequentially. Thus, if a request from the claimed second bridge arrives before the request from the claimed first bridge, the request from the second bridge will go first. Likewise, if a request from the first bridge arrives first, followed by a request from the second bridge, the request from the first bridge will go first. It is only when the two requests from the first bridge and second bridge arrive at the same time that the giving of priority is necessary. There is nothing to give priority to unless the

requests are simultaneous. Therefore, it is a requirement for the giving of priority that the requests come in at the same time.

Applicants also argued that, in view of the Examiner's acknowledgement that Sefidvash and Fujimori did not teach this kind of priority from an arbiter in the context of the claimed invention, the claims should be patentable. In response, the Examiner has cited USP 6,859,614 (Cho) for the proposition that an arbiter allows several devices simultaneously requesting access to a memory according to a predetermined priority order (referring to the abstract of Cho).

Unlike the present invention, which is directed to an IEEE 802.3 compliant physical layer device, Cho is directed to memory access in a system decoder of a DVD player. Applicants note that, while the Examiner has read the claimed arbiter on the DOM sequencer 14 in Fig. 4 of Sefidvash, nothing in Sefidvash indicates that that sequencer is giving priority to either element 11 (2-wire master controller) which the Examiner has alleged corresponds to the claimed second bridge, or element 12 (MDIO interface logic), which the Examiner has alleged corresponds to the claimed first bridge. Cho's only reference to the sequencer 14 is at col. 6, lines 32-34, which says merely that elements 11 and 12 communicate with each other through sequencer 14. There is nothing in Cho about what sequencer 14 does with communications from elements 11 and 12, where the sequencer 14 sends those communications, in what order it sends those communications, etc.

Without more, Applicants do not see how the Examiner can infer that the sequencer 14 is the claimed arbiter. Therefore, Applicants submit that it is improper for the Examiner to take the teachings of Cho and lay them onto Sefidvash.

Pursuant to the foregoing, Applicants submit that the pending claims in the subject application are patentable, and that the subject application is in condition for allowance. Accordingly, Applicants earnestly solicit a Notice of Allowance.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

The Office is hereby authorized to charge any fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,
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